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EXAMINER	
VENT, JAMIE J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,029	HOLZMANN ET AL.	
	Examiner	Art Unit	
	Jamie Vent	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable by Wong et al (U.S 5,745,409) in view of Prater (US 6,429,237) in further view of Roza (U.S. 6,087,968).

[Claim 1]

In regard to claim 1, Wong et al discloses a method of recording a digital analog voice signal sampled at a first rate and analog signal, comprising:

- sampling said analog signal at a second rate different from the first rate to form a first set of discrete analog samples(Figure 3A shows an analog input 110 and an analog input buffer connected to a sample and hole circuit 120 via MUX 330);
- storing said first set of discrete analog samples into a first set of respective cells of a memory array (Figure 3A shows a

digital/analog memory array 190 connected to an analog write circuit 125. column 5, line 56-67 and column 6 line 1-3 further describes the analog signal recording method);

- sampling said continuous-time analog signal at the second rate to form a second set of discrete analog samples (Figure 3A shows the a digital to analog converter 310 connected to the sample and hold circuit 120 via MUX 330); and
- storing said second set of discrete analog samples into a second set of respective cells of said memory array (Figure 3A shows a digital/analog memory array 190 connected to an analog write circuit 125. column 9, line 54-67 and column 10, line 1-5 further describes the digital signal recording method); however fails to specifically state converting said digital analog voice signal into a continuous-time analog signal.

Prater discloses a digital to analog converter wherein converting said digital signal into a continuous-time analog signal. Generating of a pulse-width signal allows for filtering of the pulse-width modulated signal to form a continuous-time analog signal as seen in Figure 4, Digital Sigma-Delta and described in Column 5 Lines 60+ to Column 6 Lines 1-9. Roza discloses duty cycle of the modulated signal depends on the input signal (column 2, line 25-29). Thereby, the modulated signal can be asynchronous with the input signal to produce greater accuracy of conversion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the

digital to analog signal conversion method, disclosed by Prater, and the duty cycle dependency method, discloses Roza, and incorporate the digital to analog converter, disclosed by Wong et al, to reduce error during digital to analog signal conversion.

[Claim 2, 11]

In regard to claim 2, 11, Wong et al discloses a Digital to Analog converter 310; however, Wong et al fails to disclose the converting method for converting digital signal into a continuous-time analog signal. Prater discloses a digital to analog converter wherein converting said digital signal into a continuous-time analog signal comprises:

- generating a pulse-width modulated signal (Figure 4, Digital Sigma-Delta, column 5, line 60 to column 6 line 1-9); and
- filtering said pulse-width modulated signal to from said continuous-time analog signal(Figure 4 switched capacitor filter 414, column 5, line 60 to column 6, line 1-9);

However, Prater in view of Wong fails to disclose the duty cycle of the modulated signal depends on respective sample levels of said digital signal. Roza discloses duty cycle of the modulated signal depends on the input signal (column 2, line 25-29). Thereby, the modulated signal can be asynchronous with the input signal to produce greater accuracy of conversion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog signal conversion method, disclosed by Prater, and the duty cycle dependency method, discloses Roza, and incorporate the digital to analog converter, disclosed by Wong et al, to reduce error during digital to analog signal conversion.

[Claim 3,12]

In regard to claim 3 and 12 Wong et al discloses a Digital to Analog converter 310. However, Wong et al fails to disclose the converting method for converting digital signal into a continuous-time analog signal. Prater discloses a digital to analog converter, wherein converting said digital signal into a continuous-time analog signal further comprises reducing a sampling resolution of said digital signal prior to generating said pulse-width modulated signal (Figure 2 Interpolation Filter 202, column 4, line 55-66). Thereby, the conversion procedure is simplified as less digital signal is used. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog converter, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to simplify the digital to analog conversion procedure to achieve fast conversion rate.

[Claim 4]

In regard to claim 4, Wong et al discloses a Digital to Analog converter 310. However, Wong et al fails to disclose the converting method for converting digital signal into a continuous-time analog signal. Prater discloses a digital to analog converter comprising decompressing said digital signal prior to converting said digital signal into a continuous-time analog signal (Figure 4 shows a FIR or IIR filter 406, column 5, line 42-44). Thereby, compensate the non-ideal frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog converter, disclosed by Wong et al, and incorporate the

method, as disclosed by Prater, to closely approximates an ideal frequency response of the transducer system, so the overall system can be more robust.

[Claim 5]

In regard to claim 5, Wong et al discloses a method of generating a digital signal and analog signal, comprising:

- retrieving a first set of discrete analog samples from a memory array(Figure 3A shows an analog read circuit 175 connected to the digital/analog memory array via the column decoder 180);
- filtering said first set of discrete analog samples to generate said analog signal(Figure 3A shows the a sample and hold circuit 170 connected to the analog read circuit 175. Column 6, line 4-16 further describes the analog play back method);
- retrieving a second set of discrete analog samples from said memory array(Figure 3A shows an analog read circuit 175 connected to the digital/analog memory array via the column decoder 180);
- filtering said second set of discrete analog samples to generate a continuous-time analog signal (Figure 3A shows the a sample and hold circuit 170 connected to the analog read circuit 175); and
- converting said continuous-time analog signal into said digital signal (Figure 3A shows a analog to digital convert 390 connected to the sample and hold circuit. Column 6, line 51-62 further describes the digital playback method)

[Claim 6, 15]

In regard to claim 6 and 15, Wong et al discloses converting said continuous-time analog signal into said digital signal comprises: generating discrete samples of said continuous-time analog signal (Figure 3A shows a sample and hold circuit 170 connects to an analog read circuit 175); however, Wong et al fails to discloses the generating a pulse-with modulated signal whose duty cycle respectively depends on the amplitude of said discrete samples of said continuous-time analog signal; and also fail to discloses digitizing the pulse-width modulated signal. Prater discloses information about generating a pulse-width modulated signal and the pulse-width modulated signal is digitized (Figure 5 shows a Analog Sigma-Delta modulator 506 connected to 508 where the signal is digitized. Column 6, line 57-65); however, Prater fails to disclose the duty cycle of the modulated signal depends on respective sample levels of said digital signal. Roza discloses duty cycle of the modulated signal depends on the input signal (column 2, line 25-29). Thereby, the modulated signal can be asynchronous with the input signal to produce greater accuracy of conversion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog signal conversion method, disclosed by Prater, and the duty cycle dependency method, discloses Roza, and incorporate the converting method, disclosed by Wong et al, to reduce error during digital to analog signal conversion.

[Claim 7,16]

In regard to claim 7 and 16, Wong et al discloses generating discrete samples of said continuous-time analog signal comprises generating said discrete samples that

comprises an voltage of continuous-time analog signal between respective samples (column 7, line 39-45). However, Wong et al fail to disclose the average voltage of said continuous-time analog signal between respective samples. Prater discloses the average voltage of said continuous-time analog signal between respective samples (Figure 2 shows a interpolation Filter 202). Thereby, less information can be stored into memory. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the signal generation method, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to reduce the amount of information saved into memory and thereby proving a cost efficient system.

[Claim 8, 17]

In regard to claim 8 and 17, Wong et al discloses information about converting said continuous-time analog signal into digital signal. However, Wong et al fails to discloses information about increasing a sampling resolution of said digital signal. Prater discloses converting said continuous-time analog signal into digital signal comprises increasing a sampling resolution of said digital signal (Figure 2 shows a decimation filter 204 which can be used to increased the sampling resolution). Thereby, less distortion is produced. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the signal converting method, disclosed by Prater, and incorporate the method, as disclosed by Wong, to minimize noise and reduce distortion so the performance of the overall system increases.

[Claim 9, 18]

In regard to claim 9 and 18, Wong et al discloses information about converting said continuous-time analog signal into digital signal. However, Wong et al fails to discloses information about compressing said digital signal. Prater discloses converting said continuous-time analog signal into said digital signal comprises compressing said digital signal. (Figure 2 decimation filter, column 4, line 39-43). Thereby, less noise is produced. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the signal converting method, disclosed by Prater, and incorporate the method, as disclosed by Wong, to minimize noise and reduce distortion so the performance of the overall system increases.

[Claim 10]

In regard to claim 10, Wong et al. discloses a method of recording a digital signal, comprising:

- converting said digital signal into a continuous-time analog signal (Figure 3A shows a digital to analog converter 310 connected to the digital input/output buffers);
- sampling said continuous-time analog signal to form a plurality of discrete analog samples (Figure 3A shows the a digital to analog converter 310 connected to the sample and hold circuit 120 via MUX 330); and
- storing said plurality of discrete analog samples into respective cells of a memory array (Figure 3A shows a digital/analog memory array 190 connected to an analog write circuit 125. column 9, line 54-67 and column 10, line 1-5 further describes the digital signal recording method).

[Claim 13]

In regard to claim 13, Wong et al discloses a Digital to Analog converter 310. However, Wong et al fails to disclose the converting method for converting digital signal into a continuous-time analog signal. Prater discloses a digital to analog converter comprising decompressing said digital signal prior to converting said digital signal into a continuous-time analog signal (Figure 4 shows a FIR or IIR filter 406, column 5, line 42-44). Thereby, compensate the non-ideal frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog converter, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to closely approximates an ideal frequency response of the transducer system, so the overall system can be more robust.

[Claim 14]

In regard to claim 14, Wong et al discloses a method of generating a digital signal, comprising:

- retrieving a plurality of discrete analog samples from a memory array(Figure 3A shows an analog read circuit 185 connected to the digital/analog memory array via column decoder 180);
- generating a continuous-time analog signal from said plurality of said discrete analog sample(Figure 3A shows a sample and hold circuit 170 connected to the analog read circuit 175); and
- converting said continuous-time analog signal into said digital signal(Figure 3A shows a analog to digital converter 380 connected to the

sample and hold circuit 170. Column 6, line 51-62 further describes the method of generating a digital signal).

[Claim 19]

In regard to claim 19, Wong et al discloses an analog/digital recording system, comprising:

- a memory army(Figure 3A shows a digital/analog memory array 190);
- a converter to convert a digital signal into a continuous-time analog signal(Figure 3A shows a path, which converts a digital signal into a continuous-time analog signal, contain a digital input/output buffers 140, digital to analog converter 310); and
- a programming device to generate a first set of discrete analog samples of said continuous-time analog signal(Figure 3A shows a programming device, the sample and hold circuit 120); and
- store said first set of discrete analog samples into said memory array(Figure 3A shows the analog write circuit 125 connected to the digital/analog memory array 190 via column decoder 180); and
- generate a second set of discrete analog samples from an input analog signal(Figure 3A shows an analog input buffer 115 connected to the sample and hold circuit 120 via MUX 392); and
- store said second set of discrete analog samples into said memory array(Figure 3A shows the analog write circuit 125 connected to the digital/analog memory array 190 via column decoder 180. column 5, line

56-67, column 6, line 1-3, column 9, line 54-67, and column 10, line 1-5 further describes the analog/digital signal recording).

[Claim 20, 28]

In regard to claim 20 and 28, Wong et al discloses an analog/digital recording system; however, Wong et al fails to disclose the interior circuit of the converter. Prater discloses an analog/digital recording system, wherein converter comprises:

- a digital demodulator to generate a pulse-width modulated signal (Figure 4, Digital Sigma-Delta, column 5, line 60 to column 6 line 1-9); and
- filtering said pulse-width modulated signal to from said continuous-time analog signal(Figure 4 switched capacitor filter 414, column 5, line 60 to column 6, line 1-9);

However, Prater fails to disclose the duty cycle of the modulated signal depends on respective sample levels of said digital signal. Roza discloses duty cycle of the modulated signal depends on the input signal (column 2, line 25-29). Thereby, the modulated signal can be asynchronous with the input signal to produce greater accuracy of conversion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog signal conversion method, disclosed by Prater, and the duty cycle dependency method, discloses Roza, and incorporate the digital to analog converter, disclosed by Wong et al, to reduce error during digital to analog signal conversion.

[Claim 21, 29]

In regard to claim 21 and 29, Wong et al discloses an analog/digital recording system. However, Wong et al fails to disclose the interior circuitry of the converter. Prater discloses a analog/digital recording system, wherein converter comprises a digital smoothing interpolation filter to reduce a sampling solution of said digital signal (Figure 2 Interpolation Filter 202, column 4, line 55-66). Thereby, the conversion procedure is simplified as less digital signal is used. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog converter, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to simplify the digital to analog conversion procedure to achieve fast conversion rate.

[Claim 22, 30]

In regard to claim 22 and 30, Wong et al discloses an analog/digital recording system. However, Wong et al fails to disclose the interior circuitry of the converter. Prater discloses an analog/digital recording system, wherein converter comprising an expander to decompress said digital signal prior to converting said digital signal into a continuous-time analog signal (Figure 4 shows a FIR or IIR filter 406, column 5, line 42-44). Thereby, compensate the non-ideal frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the digital to analog converter, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to closely approximates an ideal frequency response of the transducer system, so the overall system can be more robust.

[Claim 23]

In regard to claim 23, Wong et al discloses an analog/digital playback system, comprising:

- a memory array to store first and second sets of analog samples(Figure 3A shows a digital/analog memory array 190);
- a reading device to retrieve said first and second sets of analog samples(Figure 3A shows a analog read circuit 175); and
- generate first and second continuous-time analog signal respectively from said first and second sets of analog samples(Figure 3A shows a sample and hold circuit 170 with one side connected to the analog read circuit 175 and the other side connected to the analog to digital converter 380 and the analog output buffer 165 via MUX 393); and
- a converter to convert said first continuous-time analog signal into a digital signal (Figure 3A shows the analog to digital converter 380 with one side connected to the sample and hold circuit and the other side connected to the digital input/output buffers 145 via MUX 350. Column 6, line 4-16 and line 51-61 further describes the analog/digital playback system).

[Claim 24, 32]

In regard to claim 24 and 32, Wong et al discloses an analog/digital playback system, wherein said a sample and hold circuit generate discrete samples of said continuous-time analog signal (Figure 3A shows a sample and hold circuit 170); however, Wong et al fails to disclose a switch capacitor amplifier and an analog modulator. Prater discloses a converter comprises a switch capacitor amplifier (Figure 4 shows a switched

capacitor filter 414) and an analog modulator (Figure 2 shows a digital sigma-delta modulator 210). However, Prater fails to disclose the duty cycle of the modulated signal depends on the amplitude of respective discrete samples of said continuous-time analog signal. Roza discloses duty cycle of the modulated signal depends on the input signal (column 2, line 25-29). Thereby, the modulated signal can be asynchronous with the input signal to produce greater accuracy of conversion. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the converter, disclosed by Prater, and the duty cycle dependency, discloses Roza, and incorporate the analog/digital playback system, disclosed by Wong et al, to reduce error during digital to analog signal conversion.

[Claim 25, 33]

In regard to claim 25 and 33, Wong et al discloses an analog/digital playback system. However, Wong et al fails to disclose a digital anti-aliasing decimation filter to increase a sampling resolution of said digital signal. Prater discloses converter comprises a digital anti-aliasing decimation filter to increase a sampling resolution of said digital signal (Figure 2 shows a decimation filter 204 which can be used to increased the sampling resolution and an analog filtering stage for anti-aliasing). Thereby, less distortion is produced. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the signal converting method, disclosed by Prater, and incorporate the method, as disclosed by Wong, to minimize noise and reduce distortion so the performance of the overall system increases.

[Claim 26, 34]

In regard to claim 26 and 34, Wong et al discloses an analog/digital playback system. However, Wong et al fails to disclose a compressor to compress said digital signal Prater discloses converter comprises a compressor to compress said digital signal (Figure 2 shows a shows a Analog to digital path. Column 4, line 31-43). Thereby, compensate the non-ideal frequency response. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the analog/digital playback system, disclosed by Wong et al, and incorporate the method, as disclosed by Prater, to closely approximates an ideal frequency response of the transducer system, so the overall system can be more robust.

[Claim 27]

In regard to claim 27, Wong et al discloses a digital recording system, comprising:

- a memory array(Figure 3A shows a memory array 190);
- a converter to convert a digital signal into a continuous-time analog signal(Figure 3A shows a digital to analog converter 310); and
- a programming device to generate discrete analog samples of said continuous-time analog signal(Figure 3A shows a programming device, the sample and hold circuit 120); and
- store said discrete analog samples into said memory array(Figure 3A shows the sample and hold circuit 120 connected the analog write circuit 125, and the analog write circuit is connected to the digital/analog memory array 190 via the column decoder 391. The digital recording system is further described in column 9, line 54-67).

[Claim 31]

In regard to claim 31, Wong et al discloses a digital playback system, comprising:

- a memory array to store a plurality of analog samples(Figure 3A shows a memory array 190);
- a reading device to retrieve said plurality of analog samples(Figure 3A shows a analog read circuit 175);
- generating a continuous-time analog signal from said plurality of analog samples(Figure 3A shows a sample and hold circuit. The sample and hold circuit is further described in column 6, line 11-14); and a converter to convert said continuous-time analog signal into a digital signal(Figure 3A shows a analog to digital converter 380.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamie Vent whose telephone number is 571-272-7384. The examiner can normally be reached on 7:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached on 571-272-7950. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jamie Vent
02/02/06

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